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Appl. No. 10/661,793
Appeal Brief dated 04/28/2009

Attorney Docket No.: TS01-1037
N1085-90149

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Chi-An Kao et al.**

Examiner: **Khiem D. Nguyen**

Serial No.: **10/661,793**

Group Art Unit: **2823**

Filed: **09/12/2003**

Confirmation No.: **8353**

For: **CONSTANT AND REDUCIBLE HOLE BOTTOM CD IN VARIABLE POST-CMP THICKNESS AND AFTER-DEVELOPMENT-INSPECTION CD**

CERTIFICATE OF MAILING/FACSIMILE TRANSMISSION PURSUANT TO 37 C.F.R. §1.8

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Date: April 28, 2009

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AMENDED APPEAL BRIEF – 37 CFR § 41.37

Commissioner:

This is responsive to the Notification of Non-Compliant Appeal Brief mailed April 3, 2009 in response to the Appeal Brief filed February 18, 2009 and represents an appeal from the Final Rejection of claims in the above-identified application, as made in the final Office action dated July 2, 2008 and the Advisory Action mailed September 24, 2008.

This filing is further to the Pre-Appeal Brief Request for Review filed October 31, 2008 and responsive to the Notice of Panel Decision from Pre-Appeal Brief Review mailed December 18, 2008.

The fee for filing an Appeal Brief under 37 CFR § 41.20(b)(2) was paid on February 18, 2009 in the amount of $540.00. This *AMENDED APPEAL BRIEF* is being filed in accordance with 37 CFR § 41.37, and is timely filed within One Month of the April 3, 2009 mailing date of the Notification of Non-Compliant Appeal Brief.

1. REAL PARTY IN INTEREST

The real party in interest is Taiwan Semiconductor Manufacturing Company, Ltd. The rights to this application were originally assigned to Taiwan Semiconductor Manufacturing Company, Ltd., and that assignment recorded at Reel 014502/Frame 0019.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the present appeal, that are known to Appellants or Appellants' attorney.

3. STATUS OF CLAIMS

Claims 8-17 are pending in this application with claims 8-11 and 15-17 having been rejected. Claims 12-14 were allowed. The rejection of each of claims **8-11** and **15-17** is hereby appealed.

4. STATUS OF AMENDMENTS

No amendments were filed after the final Office action of July 2, 2008. A response to the final Office action titled Response to Office Action Dated July 2, 2008 / Request for Reconsideration, was filed on August 29, 2008 and included Appellants' arguments, but did not include claim amendments. The Advisory Action dated September 29, 2008 actually indicates that the "proposed amendment(s) . . . will be entered", though no amendments were in fact filed.

Arguments were also presented in the Pre-Appeal Brief Request for Review filed October 31, 2008.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The invention relates to the fabrication of integrated circuit devices and more particularly to methods for patterning etch resist material, i.e., photoresist and for forming openings in layers such as dielectric layers that underlie the etch resist material layer. The invention provides real-time feedback loops that dynamically control both the dimensions of the features formed in the etch resist material layer and the dimensions of the openings formed in the underlying layers.

The invention is described generally in the specification from page 5, line 1 through page 6, line 10 and also in the specification on page 7, line 5 through page 25.

Integrated circuits, also broadly referred to as semiconductor devices, are formed by producing a succession of material layers over a wafer or substrate and utilizing the material layers for various purposes. Many of the material layers are patterned and this generally occurs by forming a layer photoresist over the material layer, then forming an opening in the photoresist layer. The photoresist layer is used as an etch resistant "mask" layer and openings are formed in the subjacent layer using the mask layer, typically by etching. The openings formed in the subjacent material layer generally correspond to the openings in the pattern formed in the photoresist layer and include dimensions influenced by the dimensions of the corresponding opening formed in the patterned etch resist layer. It is of critical importance to control the dimensions of both the features, e.g., openings formed in the photoresist layer and similarly the features such as openings formed in the subjacent material layer. For each layer, measurements are made of the critical dimensions, such measurements commonly abbreviated as CD's. A photolithographic process followed by a develop process is used to pattern, i.e., form openings in, the photoresist layer: hence, the critical dimensions of the etch resist layer are referred to as "after develop inspect" ADI-CD's. The openings formed by etching in the underlying layer, are usually referred to as "after etch inspect" AEI-CD's, or "after clean inspect" ACI-CD's.

The invention provides for both monitoring and controlling the critical dimensions of the etch resist, i.e., photoresist, layer and also for monitoring and controlling the

critical dimensions of openings formed in an underlying layer of insulation material, on a real-time basis.

Each of the independent claims recites, among other features, the feature of the control of the critical dimensions of the patterned layer of etch resist material. The invention provides for *controlling* the critical dimensions of the opening formed in the layer of etch resist material by *communicating* with the systems that actually produce the pattern in the photoresist layer and which are therefore responsible for the critical dimensions in the photoresist, i.e. etch resist, layer. Corrections are implemented via communication with the lithography tools, i.e. the means for creating an opening through a layer of etch resist material, to control the critical dimensions and assure that they are within specification limits.

The *means, including the feedback mechanism, for assuring that the obtained critical dimension measurement of the opening created through the layer of etch resist material is within design specification*[1] as in claims 8, 15 and 16, is described in the specification, at least on page 12, line 18 through page 14, line 7 and on page 16, line 15 through page 17, line 12 and illustrated in FIG. 3A. FIG. 3A of the specification shows evaluation sub-system 42 communicating via software link/feedback line 44 to entry point 32 of the photoresist control function 30 which includes adjustment sub-system 34 that controls the critical dimension by providing corrections in the photo system. In particular, parameters of adjustment sub-system 34 are provided via software interface 35 to the process sub-system 36 (page 12, line 21 – page 13, line 2) which applies the data in order to create an opening through a layer of photoresist. This control and correction feature is further generally described at least on page 17, lines 7-13.

The means for creating an opening through a layer of etch resist material is shown as section 15 of FIG. 1 and photoresist function 30 of FIG. 3A. Section 15 is described on page 8 which includes steps that comprise the means for creating an

[1] Stated generally: Claims 8, 15 and 16 are individually addressed, infra.

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